Assignment 0424a
The core, fundamental memory management algorithms are ultimately fairly simple, so you should set this one for a quick turnaround. To help you along, starter code has been provided on the course web site so that you can just fill in the blanks.

Outcomes
This assignment will affect your proficiency measures for outcomes 1e, 3f, and 4a–4f.

Not for Submission
By April 19
This assignment is actually short enough to be done over the weekend, so ideally you should finish this by April 19. The “official” April 24 deadline is merely a courtesy concession :)
As for reading, details on deadlocks can be found in SGG chapter 7, and memory management is covered by SGG chapters 8–9 in greater detail.

For Submission
Memory Management Algorithms
1. Implement logical-to-physical paged memory address translation. To get you started, test harness and header files have been provided on the course website.
2. Implement either the FIFO or LRU virtual memory page replacement algorithm (this is a reduced version of SGG exercise 9.40). As with the paged address translation program above, test harness and header files have been provided on the course website.

Extra Credit
You will get automatic +’s in both 1e and 3f if you successfully implement both FIFO and LRU algorithms for the second program.